Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended). A boundary scan interface circuit for ~~use with a test access port (TAP) controller for~~ testing ~~the state of~~ pin drivers of an IEEE 1149.1-compliant integrated circuit (IC) having a test access port (TAP) controller and a boundary scan register (BSR), said boundary scan interface circuit comprising:

a tristate pin driver that can be enabled by said BSR unless a tristate control signal from said TAP controller is asserted;

a first mode control input signal; and

~~a tristate control circuit for selectively controlling pin driver enable input of said pin drivers and responsive to a control input for temporarily de-asserting a signal that tri-states the pin drivers during a capture cycle of said TAP in which pin logic values are captured by the BSR~~

a tristate control circuit that, when said first mode control input signal is logic 1, temporarily de-asserts said tristate control signal during a capture state of said TAP controller in which pin logic values are captured by the BSR.

2. (Currently Amended). ~~An~~ A boundary scan interface circuit as defined in claim 1, further including:

a second mode control input signal; and

~~an update control circuit responsive to a second control input for generating a boundary scan cell update signal to provide a first test mode for loading test data into a boundary scan register without updating outputs of said register~~ an update control circuit that, when said second mode control

input signal is logic 1, prevents the BSR from being updated during an update state of said TAP controller and instead, delays the update to another state before said capture state.

3. Canceled.

4. (Currently Amended). ~~An~~ A boundary scan interface circuit as defined in claim 1, said tristate control circuit including:

first means for combining said first mode control input signal, a TAP controller Capture-DR state signal and a test clock signal ~~control input and producing a tristate disabling control signal~~ to produce a tristate control signal; and

second means for combining a tristating signal from said BSR and said tristate ~~disabling~~ control signal to produce a pin driver enable signal ~~for producing a pin driver enable control~~ signal.

5. (Currently Amended). ~~An~~ A boundary scan interface circuit as defined in claim 4, said ~~tristate disabling control~~ pin driver enable signal being a pulse having a duration of one clock period of a test clock.

6. (Currently Amended). ~~An~~ A boundary scan interface circuit as defined in claim 2, said update control circuit including:

first means for combining a test clock signal and a TAP controller Run-test/idle state signal ~~for producing~~ to produce a delayed update control signal; and

second means responsive to ~~a test~~ said second mode control input signal for selecting between a TAP controller Update-DR state signal and said delayed update control signal ~~for providing~~ to produce an update signal to said BSR.

7. (Currently Amended). ~~An~~ A boundary scan interface circuit as defined in claim ~~6~~18, said update control circuit including:

_____means for combining a test clock signal with one of a TAP controller run-test/idle state signal and a TAP controller select-DR state signal to produce a delayed ~~boundary scan register~~ BSR update control signal; and

_____ a selector responsive to a test mode control signal for selecting between a ~~test access port~~ TAP update signal and said delayed control signal.

8. (Withdrawn). A method for testing the function of a pin driver enable bit of unconnected pins of an integrated circuit (IC) having a boundary scan register (BSR), comprising: loading the BSR with pin driver data and enable logic values and updating BSR outputs; re-loading the BSR with data, without updating BSR latches, that would cause the output drivers to drive their opposite logic value and to tristate their outputs; applying an output driver tristating signal to tristate all pins simultaneously; updating BSR outputs; de-asserting said tristating signal and then capturing pin logic values into said BSR; and unloading captured data from said BSR and comparing captured data against expected values.

9. (Withdrawn). A method as defined in claim 8, performing said updating BSR outputs during one of a TAP Run-Test/Idle state or a TAP Select-DR state of an IEEE 1149.1 test access port (TAP).

10. (Withdrawn). A method as defined in claim 8, performing said step of de-asserting said tristating signal in response to a delayed test access port (TAP) Capture-DR signal and an active test mode control signal.

11. (Withdrawn). A method as defined in claim 8, performing said step of tristating all pins simultaneously prior to said loading the BSR with pin and pin driver enable logic values and maintaining said pins continuously tristated throughout a test and de-asserting the tristating only during a test clock period in which test connection logic values are captured by the BSR.

12. (Withdrawn). A method of testing an integrated circuit having a boundary scan register (BSR) to determine whether circuit output pins have short circuits between the pins and a power rail, or any defect that might result in the flow of excess current through the pin or a power rail, the method comprising: tristating said output pins; loading the BSR with values to force output drivers into desired output states; capturing pin outputs into said BSR while de-asserting tristating only during a capture cycle; and unloading captured data from said BSR and comparing captured data against expected values.

13. (Withdrawn). A method as defined in claim 12, further including, after said tristating said output pins, configuring said circuit in a test mode in which output pin tristating is de-asserted during a portion of a pin output capture cycle.

14. (Withdrawn). A method of testing an integrated circuit to determine whether boundary scan register (BSR) pin enable bit paths are not stuck in an "on" state, said method comprising: loading desired circuit pin data and pin driver enable data into a BSR and updating said BSR; loading opposite circuit pin data and opposite pin driver enable data into said BSR and suppressing updating of said register during a following update cycle of a test access port (TAP); forcing output drivers into a high impedance state; updating the data inputs to the output drivers to opposite logic values during one of a Run-

test/idle or a Select-DR state of said TAP; de-asserting a signal that tristates said drivers and then capturing pin logic values; and unloading and comparing captured logic values with expected logic values to determine whether any pin enable bit path is stuck in an "on" state.

15. (Withdrawn). A method as defined in claim 14, further including, prior to said loading opposite pin data, configuring the circuit in a test mode in which a pin tristating signal is de-asserted during a portion of a pin output capture cycle and BSR update is suppressed during a boundary scan update cycle and performed during a Run-test/idle or a Select-DR state of a circuit test access port.

16. (Withdrawn). A method of testing integrated circuits having a boundary scan register (BSR) to detect defects that might result in the flow of excess current, at least one integrated circuit having a tristate control circuit as defined in claim 1, said method comprising: tristating output pins of each said at least one integrated circuit having said tristate control circuit; loading the BSR of all integrated circuits with values to force output drivers into desired output states; capturing pin outputs into said BSR of all integrated circuits while de-asserting tristating only during a capture cycle of each said at least one integrated circuit; and unloading captured data from said BSR of all integrated circuits and comparing captured data against expected values.

17. (Withdrawn). A method as defined in claim 16, said steps of tristating, loading, capturing and unloading being performed using the IEEE1149.1 standard.

18. (New) A boundary scan interface circuit for use with a test access port (TAP) controller for testing the state of pin drivers of an IEEE 1149.1-

compliant integrated circuit (IC) having a boundary scan register (BSR), said interface circuit comprising:

a tristate control circuit for selectively controlling a pin driver enable input of said pin drivers and responsive to a control input for temporarily de-asserting a signal that tri-states the pin drivers during a capture cycle of said TAP in which pin logic values are captured by the BSR;

an update control circuit responsive to a second control input for generating a boundary scan cell update signal to provide a first test mode for loading test data into a boundary scan register without updating outputs of said register;

said update control circuit including means for combining a test clock signal and a TAP Run-test/idle state signal for producing a delayed update control signal; and

means responsive to a test mode control signal for selecting between a TAP Update-DR state signal and said delayed update control signal for providing an update signal to said BSR.